Synthesis of Medium Voltage dc-to-dc Converters From Low-Voltage, High-Frequency PWM Switching Converters

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***Abstract*—Low-voltage dc-to-dc power conversion is a very mature industry which uses high-frequency pulsewidth modulation (PWM) switching techniques. The passive and active components needed to build low-voltage dc-to-dc converters are highly available, affordable and constantly improving. In this paper, a very simple and systematic method of using a large number of low-voltage, high-frequency PWM converters to synthesize highly redundant, medium voltage (4–40 kV) dc-to-dc converters is presented. Theoretical and practical considerations are discussed in necessary detail and test results of an actual 10-kW, 10 kV-to-400 V, converter built from 48 low-voltage forward converters are presented. Real-time and average reduced circuit models are derived to predict the dynamical behavior of the converter and to design the feedback control loop.**

***Index Terms*—Dc circuit breaker, feedback control, high-frequency, medium voltage, Neptune power, PWM conversion, reduced average model, redundancy, stacking, reduced real-time model.**

I. Introduction

THERE has been a growing interest, in recent years, in the transmission of power up to several thousand kilometers to the bottom of the ocean floor for sub-sea cabled observatories using medium voltages of the order of 10 kV as reported in [1]–[3]. For terrestrial applications, a similar interest exists for general electric propulsion such as trains and industrial drives [4]. The technology needed to develop the 10 kV-to-400 V dc-to-dc converter for the cabled underwater observatories was developed at the Jet Propulsion Laboratory (JPL) over a period of three years and reported in [7] and [8]. The commercialization of this converter is currently underway at Alcatel [9]. This paper discusses the synthesis, modeling, and analysis of medium voltage (MV) dc-to-dc converters using a large number of high-frequency, low-voltage PWM converters. The concepts and techniques presented go considerably beyond the general intuitive idea of stacking converters which has been known for a long time but never successfully implemented in applications approaching medium *input* voltages. Issues related to cascading converters are also addressed in [5] and [6].

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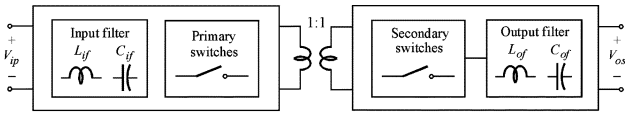


Fig. 1. Block diagram of an isolated LV converter in which the turns ratio of the isolation transformer is unity.

Among the key advantages offered by the method of synthesis presented in this paper are: a) inherent high redundancy; b) simplicity of design; c) modularity; and d) availability of components and materials. Another possible advantage, which is not discussed in this paper, is that these converters naturally act as dc circuit breakers if implemented in a dc distribution system because during a fault (short circuit, over-current, or over-voltage) the PWM drive signal to all the MOSFETs to all the converter stages can be made to vanish instantly thereby interrupting the power flow through the MV converter. Hence, the MV converters described in this work perform the functions of voltage conversion and circuit breaking simultaneously which are among the essential elements of a power distribution system.

II. Synthesis of Medium-Voltage dc-to-dc Converters From Low-Voltage Converters

A medium voltage (MV) converter is synthesized essentially by stacking a large number of isolated low-voltage (LV) converters, shown here in Fig. 1, in which the isolation transformer has a 1:1 turns ratio and is capable of withstanding the rated dc MV voltage. The choice of the LV converter topology and the method of stacking depend on the conversion ratio requirement of the MV converter. For example, for a large step-down ratio, the LV converter of choice would be a buck-derived isolated converter (full-bridge, half-bridge, two-switch forward) whose primary sides are stacked in series and secondary sides are stacked in series and parallel as shown in Fig. 2.

A convention for numbering the primary and secondary sides of an LV converter stage inside an MV converter is useful for formulating the different stacking configurations used for synthesizing a step-down, step-up, or step-up-down MV converter. An example of this convention is shown for the MV-to-LV converter in Fig. 2 where the usual *row-column* notation for a matrix is adopted. We shall refer to a column as a stack in this paper. Hence, a primary side which falls in the kth stack and jth row is denoted by (j, k) while a secondary side which falls in the lth stack and mth row is denoted by (l, m). For example, if N is the total number of LV converter stages all of whose primary sides are connected in series in a single stack as in Fig. 2, then $k = 1$

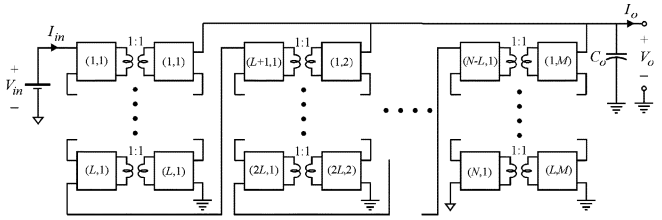


Fig. 2. An example of an MV converter designed for large step down (MV-to-LV) in which all the primary sides of the LV converters are connected in series while the secondary sides are connected in series and parallel.

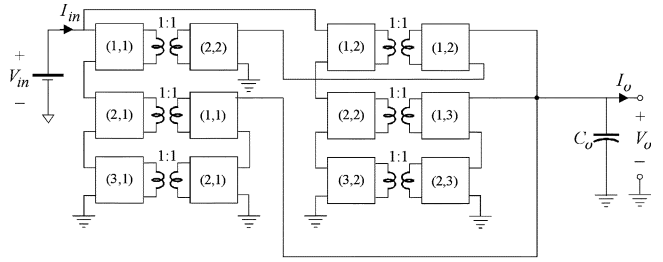


Fig. 3. Example of interlocked or irreducible stacking.

and $1 \leq j \leq N$. Also in Fig. 2, we see that on the secondary side, M stacks are connected in parallel $(1 \leq m \leq M)$, with L secondaries in each stack connected in series $(1 \leq l \leq L)$. Since the total number of LV converter stages is N, it follows that $L \times M = N$.

There are four important aspects of the synthesis of MV converter just described. First, the large number of the LV converters and the manner in which they are stacked allow the designer to achieve the required conversion ratio without relying on the turns ratio of the isolation transformer. Hence, the isolation transformer can always be designed with unity turns ratio resulting in simple construction and minimum leakage inductance. The simple construction of the isolation transformer in turn simplifies the design against the dc breakdown voltage between primary and secondary. Second, all the constituent LV converter stages are driven with the same duty cycle. Third, synchronous rectification is used to eliminate the discontinuous conduction mode. Fourth, in *each* LV converter stage, the large output or the input filter capacitor is replaced with a much smaller capacitor and a local damping network which suppresses the high frequency resonance formed by the filter inductance and the small capacitance. A *single large* capacitor is then used on the output or the input to absorb the switching current ripple as will be explained in the following sections.

There are four methods of stacking LV converters to synthesize MV converters with different conversion ratio characteristics. The following notation is introduced in this paper to represent a stacking configuration:

$$[J, K] \rightarrow [L, M] \tag{1}$$

in which

$$\begin{aligned} J &\equiv \text{Number of rows in the primary} \\ K &\equiv \text{Number of stacks in the primary} \\ L &\equiv \text{Number of rows in the secondary} \\ M &\equiv \text{Number of stacks in the secondary.} \end{aligned} \tag{2}$$

If N is the total number of LV converter stages, then we have

$$J \times K = L \times M = N \tag{3}$$

$$[J, K] = \left[J, \frac{N}{J}\right] \tag{4}$$

$$[L, M] = \left[L, \frac{N}{L}\right]. \tag{5}$$

The four methods of stacking are as follows.

1) *Simple stacking*: In this method of stacking, at least one side consists of a single stack in which all the primary or secondary sides are connected in series. The three cases for voltage conversion can be realized by the following stacking configurations:

$$\left.\begin{array}{ll} [N,1] \rightarrow \left[L, \frac{N}{L}\right], & \text{MV-to-LV} \\ \left[J, \frac{N}{J}\right] \rightarrow [N,1], & \text{LV-to-MV} \\ [N,1] \rightarrow [N,1], & \text{MV-to-MV} \end{array}\right\}. \tag{6a-c}$$

The most suitable topology of the LV converter stage for each of the three cases above will be discussed in the next three sections.

2) *Series-reducible stacking*: Although there is no apparent advantage, it is possible to stack in series several of any of the MV converter configurations in (6), each complete with its own regulated output voltage. Series reduction or decomposition of this kind of stacking can be mathematically represented by the summation symbol. For example, a series reducible MV-to-LV converter, composed of q simple-stacked MV-to-LV converters as in (6a), can be formally expanded as:

$$[qN, 1] \rightarrow \left[qL, \frac{N}{L}\right] \Rightarrow \sum_{j=1}^{q} \left\{[N,1] \rightarrow \left[L, \frac{N}{L}\right]\right\}_j. \tag{7}$$

3) *Parallel-reducible stacking*: When the power level becomes significantly high, it may be desirable to parallel several of any of the simple-stacked MV converter configurations in (6). In this case, a *single* voltage feedback is used to regulate the output voltage but the duty cycle of *each* MV converter is regulated *independently* using a current feedback loop from *each* MV converter. Parallel reduction or decomposition can be represented mathematically using the product symbol. For example, a parallel reducible MV-to-LV converter composed of q simple-stacked MV-to-LV converters as in (6a), can be formally expanded as

$$[N, q] \rightarrow \left[L, \frac{Nq}{L}\right] \Rightarrow \prod_{j=1}^{q} \left\{[N,1] \rightarrow \left[L, \frac{N}{L}\right]\right\}_j. \tag{8}$$

4) *Irreducible or interlocking stacking*: This type of stacking cannot be expanded as in (7) or (8) in terms of simple-stacked converters. An example is shown in Fig. 3 for a $[3,2] \rightarrow [2,3]$ stacking configuration. An important feature of this stacking method is that it has the high power capability of parallel-reducible stacking but does not require

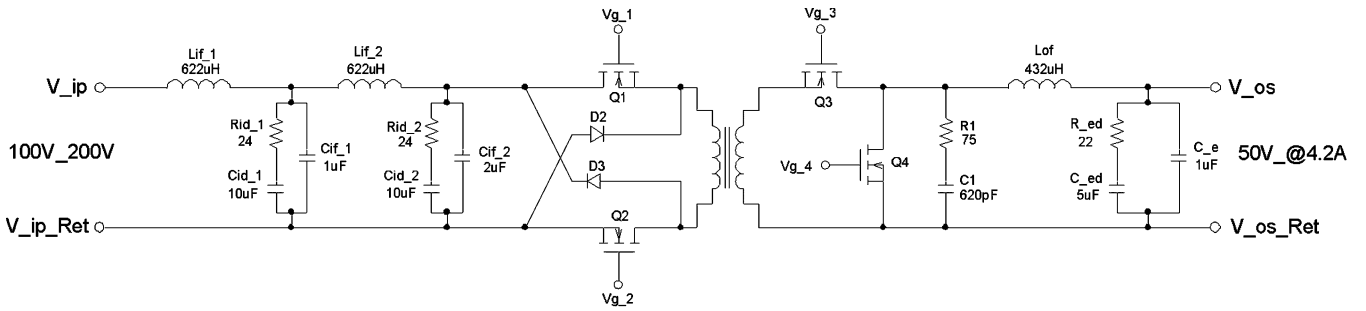


Fig. 4. Two-switch forward converter with an input filter in which the output filter capacitor is replaced with a small capacitor and a damping network. The switching frequency is 50 kHz. The values of the components shown are for the subconverter used in building the −10 kV to 400 V converter.

multiple current feedback loops to ensure current sharing among all the converters. The current is shared among all the converters naturally as a result of either the primary sides or the secondary sides being interlocked. For example, in Fig. 3, since all the converters are driven with the same duty cycle and the current on the primary side of the first stack [(1,1) through (3,1)] is the same, it follows that the current in the first stack [(1,1) and (2,1)] on the secondary side and the secondary side (2,2) are also the same. But, since (2,2) and (1,2) are in series, their currents are the same. This forces the current in the second stack on the primary side [(1,2) through (3,2)] to be the same as the current in the first stack in the primary, which in turn forces the current in the third stack on the secondary side [(1,1) and (2,1)] to be the same as the first two.

III. Synthesis of MV-to-LV Step-Down DC-to-DC Converters

An MV-to-LV step down converter is synthesized naturally by connecting the primary sides of a large number of LV converters in series and the secondary sides in a series and parallel configuration. As an illustrative example, we will determine the number of converters and their topology needed to synthesize an MV-to-LV converter which will deliver 10 kW at 400 V from a 6 kV-to-12 kV input voltage source.

Since this is a step-down application, we shall consider using the two-switch forward converter, shown in Fig. 4, in which the output filter capacitor has been removed and replaced with a small capacitor and a parallel damping branch whose element values are given by

$$C_{\varepsilon d} = \alpha C_{\varepsilon}; \quad 5 < \alpha < 10 \tag{9}$$

$$R_{\varepsilon d} = Q_{\varepsilon}\sqrt{L_{\rm of}/C_{\varepsilon}}; \quad 1.5 < Q_{\varepsilon} < 2.5. \tag{10}$$

The voltage conversion ratio of this converter stage is

$$M_v \equiv \frac{V_{\rm os}}{V_{\rm ip}} = D; \quad 0 < D < 0.5. \tag{11}$$

To determine the number of the LV converter stages needed, we shall allow the input of each stage not to exceed about 200 to 300 V. After some basic considerations, one can verify that forty-eight LV converter stages can be used by connecting them according to the following stacking configuration:

$$[J, K] \rightarrow [L, M] \Rightarrow [48, 1] \rightarrow [8, 6]. \tag{12}$$

The range of the duty cycle is acceptable to the forward converter and is given by

$$\frac{50\ \text{V}}{(12\ \text{kV}/48)} = 0.2 = D_{\min} < D < D_{\max} = \frac{50\ \text{V}}{(6\ \text{kV}/48)} = 0.40. \tag{13}$$

Each LV stage puts out $208\ \text{W} = 10\ \text{kW}/48$ at 50 V and has a maximum input voltage of $12\ \text{kV}/48 = 250$ V. Each stack on the secondary side puts out $1664\ \text{W} = 8 \times 208$ W at $8 \times 50\ \text{V} = 400$ V. At the 400-V output, a single 100 μF is used to filter the inductive current from all six stacks to provide a smooth output voltage with 250 mV peak-to-peak ripple voltage when the converter is operating at a switching frequency of 50 kHz. The voltage conversion ratio of this MV-to-LV converter is given by

$$M_V = \frac{V_o}{V_{\rm in}} = \frac{M_v}{(L/N)} = \frac{D}{(48/8)} = \frac{D}{6}. \tag{14}$$

The two-stage input filter in Fig. 4 is damped against the negative impedance loading of the converter stage. A two-stage filter is not necessary and in many cases a single stage LC filter is adequate. The worse case negative impedance loading occurs at minimum input voltage and maximum load which can be expressed as

$$R_{\rm in} = -\frac{\left(\frac{V_{\rm in\_min}}{N}\right)^2}{\frac{P_{\rm out}}{N}} = -\frac{V_{\rm in\_min}^2}{NP_{\rm out}}. \tag{15}$$

A simple rule for damping the input filter for unconditional stability is given by

$$Q_{\rm if} = \frac{R_{\rm id} \,\|\, R_{\rm in}}{\sqrt{L_{\rm if}/C_{\rm if}}} \approx 1.5. \tag{16}$$

Generally, a $Q_{\rm if}$ in the range 1.2 to 2 is acceptable. One can also fine tune the damping elements using a few CAD iterations. For a more in-depth analysis, the reader is referred to the classic work of Middlebrook in [13].

Some steady-state quantities of this converter example are computed next. The maximum peak-to-peak ripple current in the output inductor occurs at the highest input voltage ($D_{\min}$) and is given by

$$I_{r\_\rm pp} = \frac{V_o(1 - D_{\min})T_s}{L_{\rm of}} = \frac{50\ \text{V}(1 - 0.2)20\ \mu s}{432\ \mu\text{H}} = 1.86\ \text{A}. \tag{17}$$

The maximum peak-to-peak output ripple voltage is given by

$$V_{o\_r\_\mathrm{pp}} = M\frac{T_s I_{r\_pp}}{8C_o} = 6\frac{20\ \mu s 1.86\ \mathrm{A}}{8(100\ \mu\mathrm{F})} = 277\ \mathrm{mV} \tag{18}$$

where we have used the fact that the ripple current flowing into the output capacitor is the sum of the ripple current out the six output stacks ($M = 6$).

The input ripple current of a single-stage LC input filter is given by

$$\begin{aligned} I_{\mathrm{in}\_r\_\mathrm{pp}} &= \frac{I_o}{M}\left(\frac{f_{o\_\mathrm{if}}}{F_s}\right)^2 \frac{\pi^2 D_{\max}(1-D_{\max})}{2} \\ &\approx \frac{I_o}{M}\left(\frac{f_{o\_\mathrm{if}}}{F_s}\right)^2 \frac{4\sin\pi D_{\max}}{\pi} \end{aligned} \tag{19}$$

where

$$f_{o\_\mathrm{if}} = \frac{1}{2\pi\sqrt{L_{\mathrm{if}}C_{\mathrm{if}}}}. \tag{20}$$

For the two-stage LC filter, the input ripple current is given by

$$\begin{aligned} I_{\mathrm{in}\_r\_\mathrm{pp}} &\approx \frac{I_o}{M}\frac{1}{(2\pi F_s)^4}\frac{1}{L_{\mathrm{if}1}L_{\mathrm{if}2}C_{\mathrm{if}1}C_{\mathrm{if}2}}\frac{4\sin\pi D_{\max}}{\pi} \\ &= \frac{25\ \mathrm{A}}{6}\left(\frac{1}{2\pi.50\ \mathrm{kHz}}\right)^4 \\ &\quad \times \frac{1}{622\ \mu\mathrm{H}.622\ \mu\mathrm{H}.1\ \mu\mathrm{F}.2\ \mu\mathrm{F}}\frac{4\sin(\pi 0.4)}{\pi} \\ &= 670\ \mu\mathrm{A}. \end{aligned} \tag{21}$$

IV. Synthesis of LV-to-MV Step-Up dc-to-dc Converters

An LV-to-MV step-up converter is synthesized by connecting the secondary sides of a large number of LV converters in series and the primary sides in series and parallel according to the stacking configuration in (6b). As an illustrative example, we will determine the number of converters and their topology needed to synthesize an LV-to-MV converter which delivers 10 kV at 10 kW from a 200-to-400 V input voltage source.

Since this is a step-up application, the isolated boost converter topology shown in Fig. 5(a) is used whose voltage conversion ratio is given by

$$M_v = \frac{V_{\mathrm{os}}}{V_{\mathrm{ip}}} = \frac{1}{1-D}. \tag{22}$$

The duty cycle D in (22) is defined in Fig. 5(b). Because the transformer is center-tapped, the drain-to-source voltage of the MOSFETs during the off-time is twice the output voltage. If an isolation transformer without a center-tap is desired, then the variation shown in Fig. 6 is used whose voltage conversion ratio is given by

$$M_v = \frac{V_{\mathrm{os}}}{V_{\mathrm{ip}}} = \frac{4}{1-D} \tag{23}$$

in which the duty ratio is defined as before in Fig. 5(b). The reason for the appearance of the factor 4 in (23) is because of the frequency doubling action of the split inductors on the input side and the voltage doubling configuration at the output. The

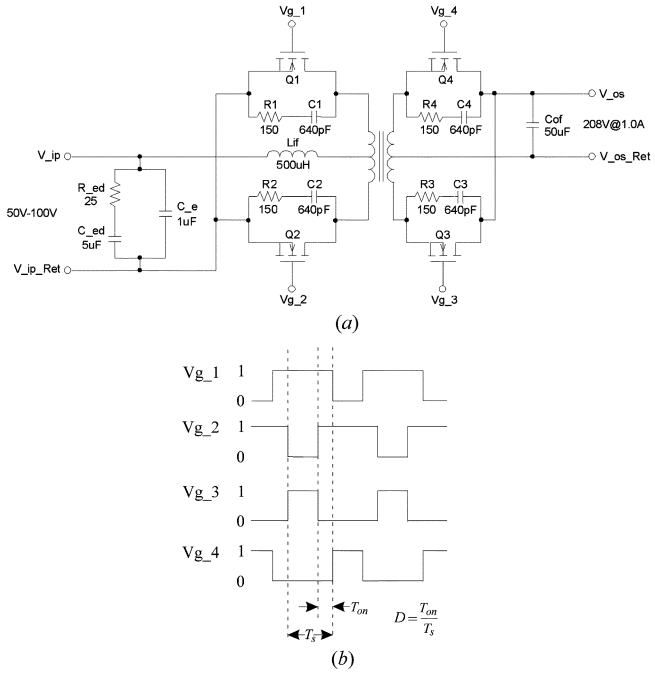


Fig. 5. (a) Isolated boost converter with a center-tapped transformer. On the input, a small capacitor with a damping network is used. (b) Gate-drive waveforms and definition of duty cycle.

drain-to-source voltage of the switches on the primary side for this topology is only half the output voltage while that of the output MOSFETs is equal to the output voltage. The smallest conversion ratio for this converter is 4.

Since the input voltage is fairly low, only a few converters are needed in a stack on the primary side to divide the input voltage. On the output side, since the voltage is high, all the converters are connected in series. According to the stacking configuration in (6b) the conversion ratio of the LV-to-MV converter is given by

$$M_V = \frac{V_o}{V_{\mathrm{in}}} = \frac{N}{J}M_v. \tag{24}$$

Hence, the desired LV-to-MV converter can now be built by stacking 48 of the converter Fig. 5(a) as follows:

$$[J,K] \rightarrow [L,M] \Rightarrow [4,12] \rightarrow [48,1]. \tag{25}$$

Each converter in this configuration delivers 208 W at an output voltage of 208 V and operates from an input voltage of 50-to-100 V. When 48 of the converters in Fig. 6 are used, then the stacking configuration becomes

$$[J,K] \rightarrow [L,M] \Rightarrow [8,6] \rightarrow [48,1]. \tag{26}$$

Each converter in this configuration delivers 208 W at an output voltage of 208 V and operates from an input voltage of 25-to-50 V.

To meet EMI requirements, a damped LC filter is added at the input of the boost converter in order to attenuate the switching current in the input inductor to an acceptable level. In Figs. 5(a) and 6, we see that the inputs of these boost converters are stripped of this additional LC filter and instead a small a capacitor, C_ε, with a damping network, $R_{\varepsilon d}, C_{\varepsilon d}$ is used. A

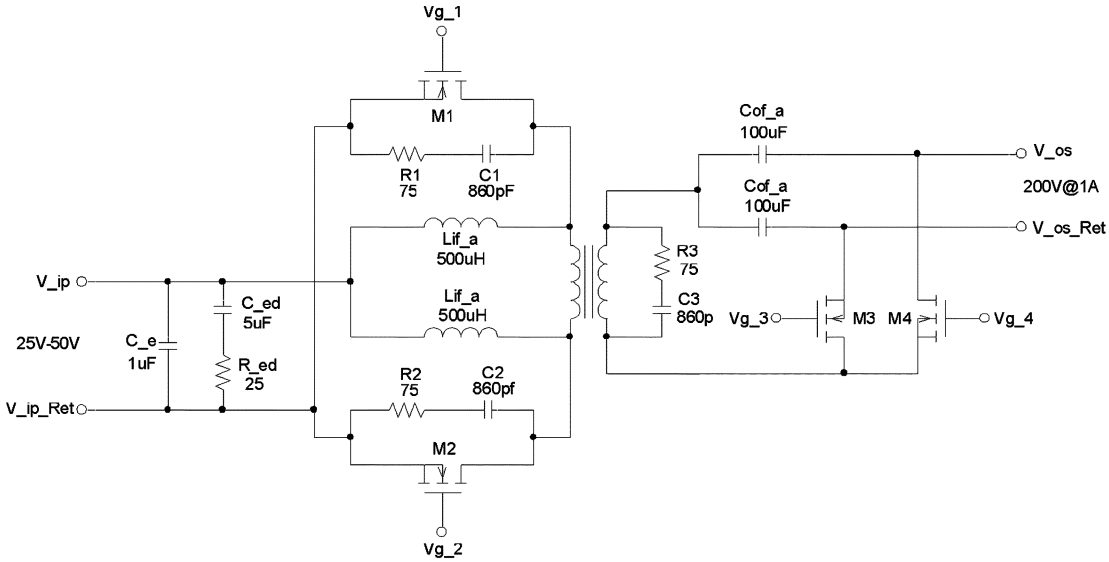


Fig. 6. Isolated boost converter without a center-tapped transformer.

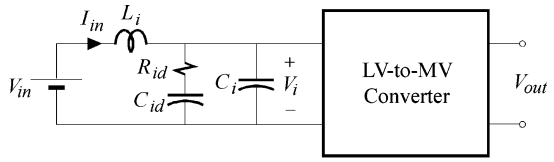


Fig. 7. Addition of a single LC filter at the input of an LV-to-MV converter.

single LC stage is then added at the input of the LV-to-MV converter as shown in Fig. 7.

The equations for the damping network $R_{\varepsilon d}, C_{\varepsilon d}$ are

$$C_{\varepsilon d} = \alpha C_{\varepsilon}, \quad 5 < \alpha < 10 \tag{27}$$

$$R_{\varepsilon d} = Q_{\varepsilon}\sqrt{L_{\rm if}/C_{\varepsilon}}, \quad 1.5 < Q_{\varepsilon} < 2.5. \tag{28}$$

The design equations for damping the input filter in Fig. 7 are

$$Q_{\rm if} = \frac{R_{\rm id} \,\|\, R_{\rm in}}{\sqrt{L_i/C_i}} \approx 1.5 \tag{29}$$

where

$$R_{\rm in} = -\frac{V_{\rm in\_min}^2}{P_{\rm in}}.$$

The values of the snubbers shown in Figs. 5(a) and 6 are for a typical leakage inductance of 3–5 μH and a frequency of operation of 50 kHz.

Some additional basic steady state voltages and currents of this converter example are given next. The peak-to-peak ripple current in the input inductor, $L_{\rm if}$, is given by

$$I_{r\_\rm pp} = \frac{V_o}{NL_{\rm if}F_s}D(1-D). \tag{30}$$

The maximum peak-to-peak output voltage ripple is given by

$$V_{o\_r\_\rm pp} = NI_{o_{\max}}\frac{D_{\max}}{C_{\rm of}} \tag{31}$$

in which

$$C_{\rm of} = \begin{cases} C_{\rm of}, & \text{Fig. 5a} \\ C_{of\_a}/2, & \text{Fig. 6} \end{cases}. \tag{32}$$

The peak-to-peak input ripple current drawn from the input voltage source is given by

$$I_{{\rm in}\_r\_\rm pp} = \frac{1}{L_iL_{\rm if}C_i}\frac{1}{2\pi^4F_s^3}\frac{V_o}{J}\sin\pi D. \tag{33}$$

V. Synthesis of MV-to-MV dc-to-dc Converters

An MV-to-MV step-up-and-down converter is synthesized by connecting the secondary and the primary sides of a large number of LV converters in series according to the stacking configuration in (6c). As an illustrative example, we will determine the number of converters and their topology needed to synthesize an MV-to-MV converter which delivers 10 kV at 10 kW from a 7-to-13 kV input voltage source. Although the sepic and the zeta converters can be used in this application, the most suitable topology with the simplest isolation transformer design is the uncoupled Cuk converter [10] shown here in Fig. 8. The MV-to-MV converter synthesized from the Cuk converter and the Cuk converter have the same voltage conversion ratio which is given by

$$M_V = M_v = \frac{D}{D'}. \tag{34}$$

The input current of the Cuk converter is the same as that of the boost converter and needs an additional input filter. Since the input voltage is high, the additional input LC filter is designed into each converter stage rather than at the MV input. The damping elements of input filter are determined according to (15) and (16) and given by

$$Q_{\rm if} = \frac{R_{\rm id} \,\|\, R_{\rm in}}{\sqrt{L_{\rm in}/C_{\rm in}}} \approx 1.5 \tag{35}$$

$$R_{\rm in} = -\frac{\left(\frac{V_{\rm in\_min}}{N}\right)^2}{\frac{P_{\rm out}}{N}} = -\frac{V_{\rm in\_min}^2}{NP_{\rm out}}. \tag{36}$$

The output filter of the Cuk converter is similar to the buck converter so that the large output filter capacitor is replaced with a small capacitor (1 μF in Fig. 8) and a damping branch whose

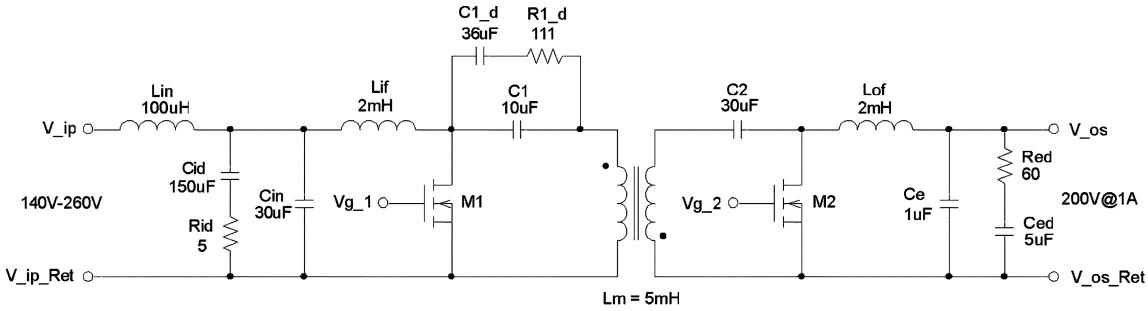


Fig. 8. Cuk converter stage with an input filter.

values are given by (9) and (10). At the output of the MV converter, a single a capacitor, C_o, is used. The purpose of the *RC* branches across C_1 is to damp out a sharp glitch in the control-to-output transfer function as discussed in detail in [14]. The capacitors C_1 and C_2 are chosen according to the glitch-removal condition

$$\frac{C_2}{C_1} = \frac{1}{D_{\text{nom}}^2} - 1 \tag{37}$$

in which D_{nom} is the value of duty cycle at the nominal input voltage. With (37) satisfied, the elements of the damping network are chosen according to

$$R_{1d} = Q_{1d}\sqrt{\frac{L_m}{C_1 + C_2}}, \quad Q_{1d} \approx 10 \tag{38}$$

$$C_{1d} = \frac{\alpha}{Q_{1d}}(C_1 + C_2), \quad \alpha = 3 \tag{39}$$

in which L_m is the magnetizing inductance the isolation transformer.

The drain-to-source voltage of the MOSFETs is equal to the sum of the input and output voltages and the drain current of each MOSFET equals to the sum of the input and output currents.

If we choose 50 converter stages, then maximum input voltage of each stage will be $13\ \text{kV}/50 = 260$ V and the output voltage will be $10\ \text{kV}/50 = 200$ V. Hence, the maximum drain-to-source voltage of the MOSFETs will be 460 V. The maximum and minimum values of the duty cycle are determined to be

$$D_{\min} = \frac{1}{1 + 1/M_{V\_\min}} = \frac{1}{1 + 13\ \text{kV}/10\ \text{kV}} = 0.437$$
$$D_{\max} = \frac{1}{1 + 1/M_{V\_\max}} = \frac{1}{1 + 7\ \text{kV}/10\ \text{kV}} = 0.588. \tag{40}$$

Some of the steady-state voltages and currents for this example are computed next. It is assumed that the converter is operating at 50 kHz. The maximum peak-to-peak ripple current in the input and output inductors are the same and is given by

$$I_{r\_\text{pp}} = \frac{V_o}{N}\frac{(1 - D_{\min})T_s}{L}, \quad L = L_{\text{if}}, L_{\text{of}}$$
$$= \frac{10\ \text{kV}}{50}\frac{(1 - 0.437)20\ \mu s}{2\ \text{mH}}$$
$$= 1.13\ \text{A}. \tag{41}$$

The peak-to-peak output voltage ripple (assuming $C_o = 1\ \mu$F) is given by

$$V_{o\_r\_\text{pp}} = \frac{T_s I_{r\_\text{pp}}}{8C_o}$$
$$= \frac{20\ \mu s 1.13\ \text{A}}{8(1\ \mu\text{F})}$$
$$= 2.83\ \text{V}. \tag{42}$$

The peak-to-peak input ripple current is given by

$$I_{\text{in}\_r\_\text{pp}} = \frac{1}{L_i L_{\text{if}} C_i}\frac{1}{2\pi^4 F_s^3}\frac{V_o}{N}\frac{\sin \pi D_{\min}}{D_{\min}}$$
$$= \frac{1}{(100\ \mu\text{H})(2\ \text{mH})(30\ \mu\text{F})}$$
$$\times \frac{1}{2\pi^4(50\ \text{kHz})^3}\frac{10\ \text{kV}}{50}\frac{\sin(\pi 0.437)}{0.437}$$
$$= 3.1\ \text{mA}. \tag{43}$$

The values of the components in this example are chosen reasonably for illustration purposes only and not for a carefully optimized design. Finally, note that the single capacitor, C_o, at the 10-kV output is equivalent to a much larger capacitance at the output of each LV converter stage which is computed by energy consideration as follows:

$$C_o(50 \times 200\ \text{V})^2 = C_o(50)^2(200\ \text{V})^2 = 2500C_o(200\ \text{V})^2.$$

VI. Design Equations for the Converter

Because of the straightforward method of synthesis, *all* the design equations of an MV converter can be ascertained from the design equations of its constituent LV converter stage without any difficulty. Fortunately, the theory and design of LV converters is a mature field and numerous papers and textbooks exist on the subject. In this paper, special attention will be given only to the dynamic modeling of an MV converter and the design of the feedback network.

VII. Mechanisms for Voltage and Current Sharing in MV Converters

There are five factors which ensure voltage and current sharing in the MV converters described here.

a) All the converter stages are identical within component tolerances.

b) All the converter stages are driven with the same duty cycle
c) Synchronous rectification is used to avoid the discontinuous conduction mode (DCM). In DCM voltage sharing may be violated under large dynamic load transients.
d) Extra loading effects on each converter stage, such as bootstrap windings for house keeping power, must be identical within component tolerances.
e) Losses in the converter stages due to elevated temperatures of components must remain relatively the same. Hence, an uneven *high* temperature distribution will result in uneven sharing of the voltages. If the temperature rise is small, the unevenness of the temperature distribution is not important.

The voltage and current sharing mechanism in all the simple and irreducible stacked MV converters is the same and will be explained in each of the three cases. In an MV-to-LV converter, with stacking configuration $[N,1] \rightarrow [L,(N/L)]$, all the primary sides are stacked in series so that the average input current and the average current in each of the primary sides are all identical

$$I_{\text{in}} = I^{p}_{(j,1)}, \quad j = 1 \ldots N. \tag{44}$$

Since all the converters stages are driven by the same duty cycle, it follows that the average output current of each secondary side of all the converters are also equal and given by

$$I^{s}_{(l,m)} = \frac{I_{\text{in}}}{D}, \quad l = 1 \ldots L \quad \text{and} \quad m = 1 \ldots \frac{N}{L}. \tag{45}$$

On the secondary side the current in each stack is the same current as the current in any one of the secondary sides. It follows the output current and the current in anyone of the output stacks or in any of the secondary sides are related by

$$I^{s}_{(l,m)} = I_o \frac{L}{N}. \tag{46}$$

It follows from (45) and (46) that the current conversion ratio is $I_o/I_{\text{in}} = N/LD$, which is consistent with the voltage conversion ratio in (14).

The mechanism for voltage sharing is explained in Fig. 9, where the state of any one of the output stacks during the off time, $D'T_s$, is shown. In this figure, we see that the instantaneous current in all the inductors is nearly identical because the capacitor at the output of each stage, C_e, is very small in comparison to the output filter capacitor, C_o, and almost none of the inductive ripple current shown flows through it. Hence, the voltages across the output filter inductors during $D'T_s$ in any one of the output stacks can be written and approximated as follows:

$$-v_j = L_{\text{of}_j} \frac{di_j}{dt} \approx L_{\text{of}_j} \frac{di}{dt} \approx L_{\text{of}} \frac{di}{dt} \tag{47}$$

where we have assumed that the output filter inductors are all nearly the same. It follows that the output voltages of the converter stages in a stack are all nearly identical during $D'T_s$

$$v_1 = v_2 = \cdots = v_L = \frac{V_o}{L}. \tag{48}$$

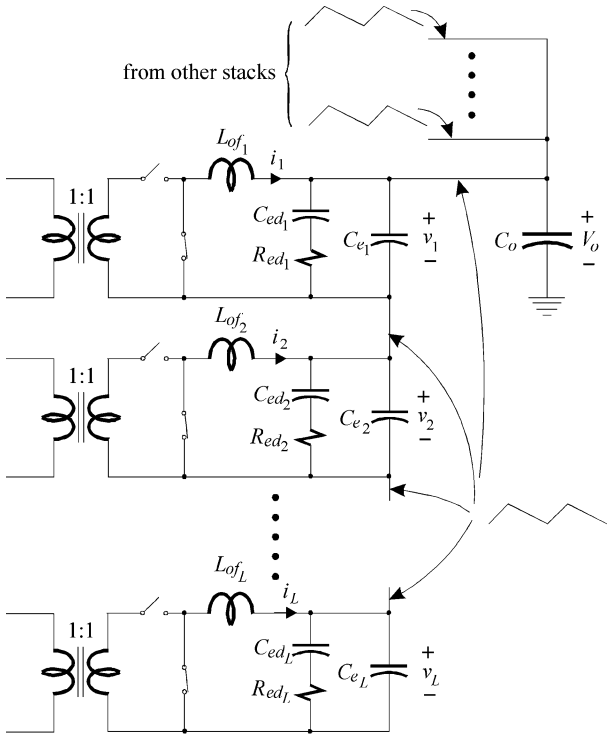


Fig. 9. Output filter inductors during the off time, $D'T_s$, in the MV-to-LV converter.

Now we have:

a) the average value of the current in all the output filter inductors is the same;
b) the slope of current in all of the output filter inductors during $D'T_s$ is the same.
c) all the output filter inductors are driven with the same DT_s and $D'T_s$.

It follows that the slope of the current in all of the output filter inductors during DT_s is also the same. This proves that not only is the average value of the current in all of the output filter inductors in a stack the same, but also the instantaneous value. Hence, the small capacitors, C_e, at the output of each converter stage maintain their identical voltages as given by (48) during DT_s because no significant differences exist in the circuit conditions amongst them during DT_s. This proves the output voltages of all the converter stages in a stack share the output voltage equally and almost instantaneously so that (48) is valid for all t and not just during $D'T_s$. Since the output voltages and currents of all the converter stages in a stack are the same, they all share the output power of the stack equally. Now, if the efficiencies of all the converters are nearly identical, then they will all also share the input power to the stack equally. It follows that the average value of the input voltage to each converter stage in the stack will be the same because the average input currents of all the converter stages is the same. Finally, we see that the instantaneous value of the input voltage of all the converter stages is nearly the same because the slope of the current in all the output filter inductors during DT_s is the same and is given by

$$v_{\text{in}_j} - v_j = L_{\text{of}_j} \frac{di_j}{dt} \approx L_{of_j} \frac{di}{dt} \approx L_{\text{of}} \frac{di}{dt}. \tag{49}$$

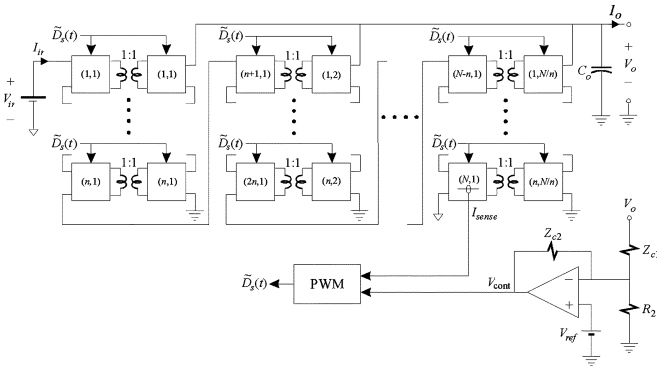


Fig. 10. Example of implementation of voltage and current feedback loops in an MV-to-LV converter.

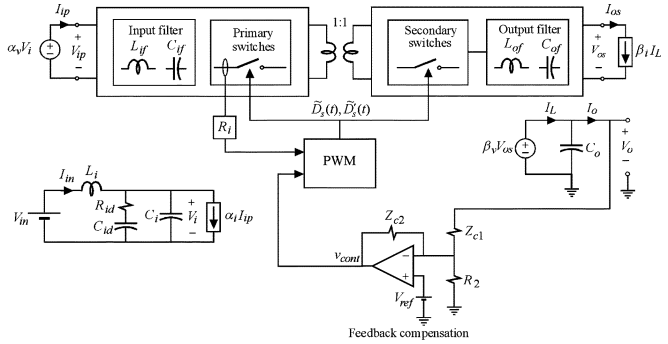


Fig. 11. General reduced circuit model for an MV-to-LV, LV-to-MV, and MV-to-MV converter.

It follows from (48) and (49) that the following is true for all t:

$$v_{\text{in}_1} = v_{\text{in}_2} = \cdots = v_{\text{in}_L} = \frac{V_{\text{in}}}{N}. \tag{50}$$

This completes the discussion of the voltage and current sharing in the MV-to-LV converter synthesized from the forward converter. The discussion for an LV-to-MV converter, synthesized from boost converters, is identical to the one for an MV-to-LV converter, synthesized from forward converters, in which the input circuit and DT_s are interchanged with the output circuit and $D'T_s$, respectively. Finally, the discussion for an MV-to-MV, converter synthesized from Cuk converters, is the same as that of an MV-to-LV converter, synthesized from forward converters, because the output circuits of the Cuk converter and the forward converter are the same. It should be noted that the original concept of implementing peak current mode control in each subconverter to regulate its duty cycle was flawed as it would cause the duty cycle to collapse or max out while the output voltage of the stack would remain regulated [11].

VIII. Feedback Control

The synthesized MV converters described above are regulated exactly in the same way as any other low-voltage PWM converter using a *single* output voltage feedback loop with an additional current feedback loop derived from the switch on the primary side of the converter. The most popular type of current feedback is peak current-mode control [15] although charge control, [19], [20], [22], and [21], can be used equally well and *may even be more suitable for MV converters because of its inherent noise immunity and superior current limiting ability*. Fig. 10 shows the voltage and current feedback loops in an MV-to-LV converter. The current is sensed on the primary side of the converter at the lowest potential to simplify the problem of isolation. For redundancy, a second or even a third current loop can be added. In the next two sections, reduced real-time and average equivalent circuit models will be given to design and predict the closed-loop behavior of these converters.

IX. Reduced Real-Time Circuit Models

In order to obtain reasonable run times for real-time simulations, a reduced circuit model of an MV converter is necessary. A general reduced model for the three types of MV converters described in this paper is shown in Fig. 11 in which the following hold.

a) The input voltage and current are scaled by two dependent sources whose gains are given by

$$\alpha_v = \begin{cases} \dfrac{1}{N}, & \text{MV}-\text{to}-\text{LV and MV}-\text{to}-\text{MV} \\ \dfrac{1}{J}, & \text{LV}-\text{to}-\text{MV} \end{cases} \tag{51}$$

$$\alpha_i = \begin{cases} 1, & \text{MV}-\text{to}-\text{LV and MV}-\text{to}-\text{MV} \\ K, & \text{LV}-\text{to}-\text{MV} \end{cases}. \tag{52}$$

b) The output voltage and current are scaled by two dependent sources whose gains are given by

$$\beta_v = \begin{cases} L, & \text{MV}-\text{to}-\text{LV} \\ N, & \text{LV}-\text{to}-\text{MV and MV}-\text{to}-\text{MV} \end{cases} \tag{53}$$

$$\beta_i = \begin{cases} \dfrac{1}{M}, & \text{MV}-\text{to}-\text{LV} \\ 1, & \text{LV}-\text{to}-\text{MV and MV}-\text{to}-\text{MV}. \end{cases} \tag{54}$$

c) The model of the LV stage is *exactly* the same as the schematic model of the LV converter used to synthesize the MV converter. Examples of schematics of LV stages were shown in Figs. 4, 5, 6, or 8.

d) The model of the control circuit, current sense and PWM circuits is *exactly* the same as the schematic model in the actual MV converter.

e) For an MV-to-LV or MV-to-MV converter, the element values for the input filter are zero $L_i = C_i = C_{\text{id}} = 0$. For an LV-to-MV converter, the values of these elements are discussed in Section IV and shown in Fig. 7.

f) For MV-to-LV and MV-to-MV converters, the value of C_o is determined according to (18) and (42) respectively and for an LV-to-MV converter, the value of this capacitor is zero, i.e., $C_o = 0$.

As a specific example, the complete real-time reduced equivalent circuit of the MV-to-LV converter ($[48, 1] \rightarrow [8, 6]$) discussed in Section III is shown in Fig. 12. The two-switch forward converter stage is modeled with high fidelity except for the details of the start-up circuits. The error amplifier, oscillator, current-sense, external ramp, comparator and PWM circuits are essentially replicas of the actual circuit used in the hardware. Note that the external ramp is subtracted from twice the control signal generated from the error amplifier instead of being added

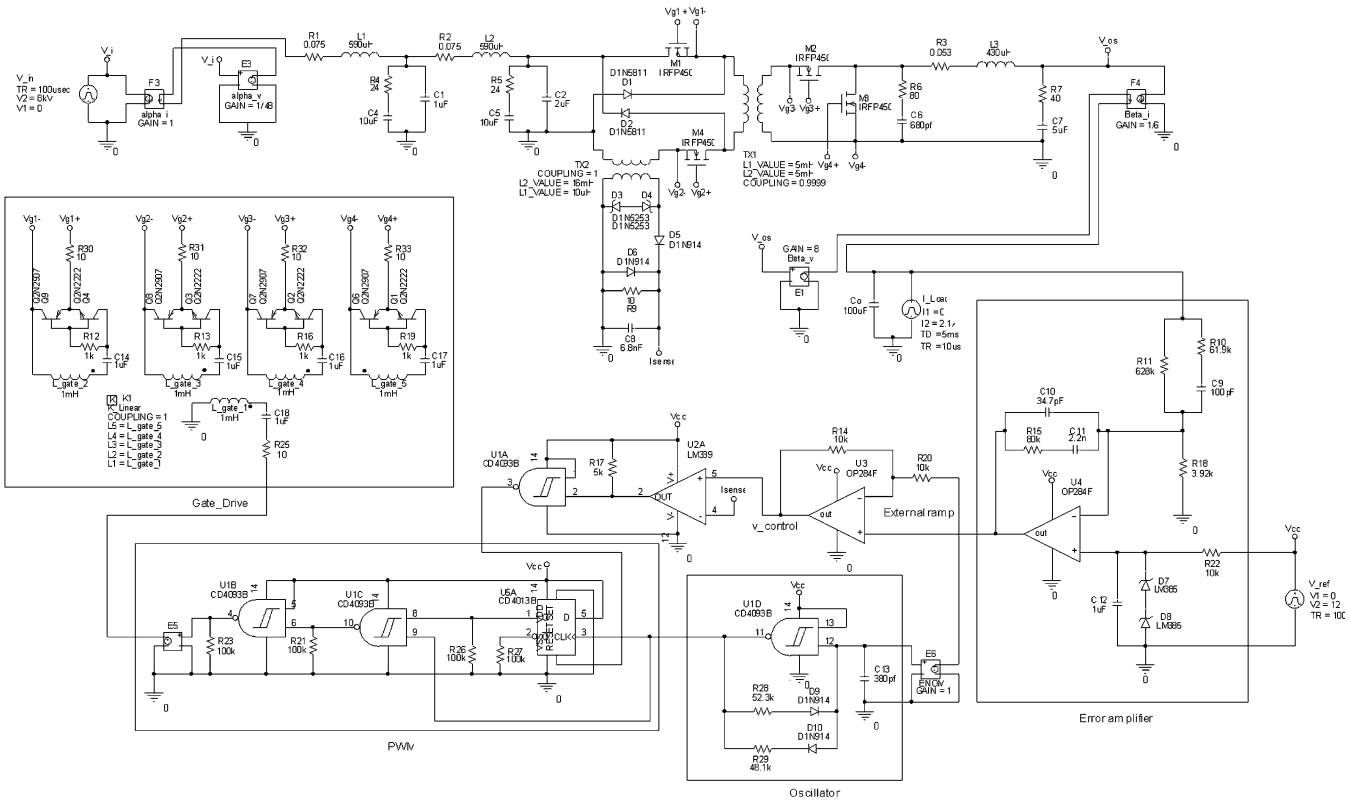


Fig. 12. Reduced real-time equivalent circuit model of the 10 kV-to-400 V converter.

to the current sense signal. The values of the scaling sources for this converter are computed to be

$$\alpha_v = \frac{1}{N}\bigg|_{N=48} = \frac{1}{48} \tag{55}$$

$$\alpha_i = 1 \tag{56}$$

$$\beta_v = L = 8 \tag{57}$$

$$\beta_i = \frac{1}{M}\bigg|_{M=6} = \frac{1}{6}. \tag{58}$$

The turns ratio of the current sense transformer is 1:40 and the value of the current sense resistor is $R_{10} = 10\ \Omega$ so that the current-to-voltage conversion trans-resistance is given by

$$R_i = \frac{R_{10}}{40} = 0.25\,\Omega. \tag{59}$$

Finally, the value of the external ramp generated by the oscillator is

$$S_e = 2.6 \times 10^5\ \mathrm{V}/s.$$

The results obtained with the model in Fig. 12 will be discussed in Section XII.

X. Reduced Average Equivalent Circuit Models

In order to design the feedback control loop of an MV converter, we need an average small-signal model of the MV converter. To do so, we substitute the PWM switch with its appropriate average small-signal model [16]–[18], and [21] in the real-time reduced model in Fig. 11. Since all simulation programs, such as Pspice, are capable of expanding any nonlinear device about a given operating point the nonlinear, *large-signal* average model of the PWM switch is normally used to simulate both the small-signal and large-signal dynamical behavior of the MV converter. The particular model of the PWM switch to be used depends on the type of feedback control used in the MV converter. Hence, if peak current-mode control is used, then one can use either the model of the current-controlled PWM switch (CC-PWM) [21] or the basic model of the PWM switch in Fig. 13 with a separate model of the current loop [17]. If charge-control is used, then one can use either use the model of the charge controlled PWM switch (QC-PWM) [21] or the basic model of the PWM switch with a separate model of the charge-control loop [20], [22]. In this paper we will demonstrate only the use of the CC-PWM switch whose large-signal and small-signal models are shown in Figs. 14 and 15, respectively.

When the appropriate model of the PWM switch is substituted in the reduced real-time model of an MV converter, we obtain an equivalent circuit model which has the general form shown in Fig. 16. The average model of the LV converter stage in Fig. 16 is shown in Fig. 17(a)–(c) for each of the LV converter stages shown earlier in Figs. 4, 5, 6, and 8.

A few explanatory notes are given for the reduced average models in Fig. 17. Although the magnetizing inductance of the isolation transformer of the forward converter in Fig. 4 does not appear in the average circuit model, it slightly modifies the

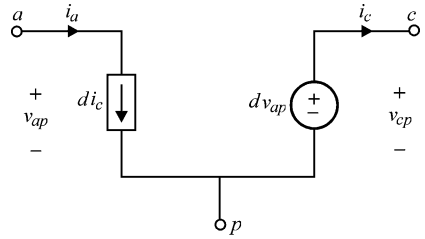


Fig. 13. Large-signal average model of the PWM switch with duty-cycle control in which the control generators are driven by the duty cycle.

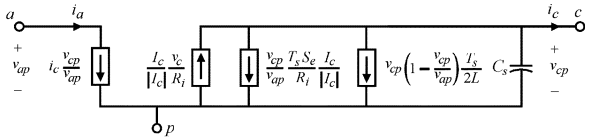


Fig. 14. Large-signal average model of the CC_PWM switch. The control generator in this model is the voltage controlled current source driven by the control signal v_c.

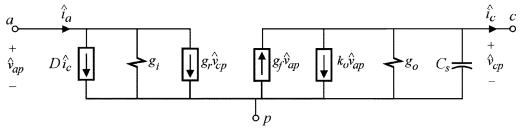


Fig. 15. Small-signal model of the CC-PWM switch.

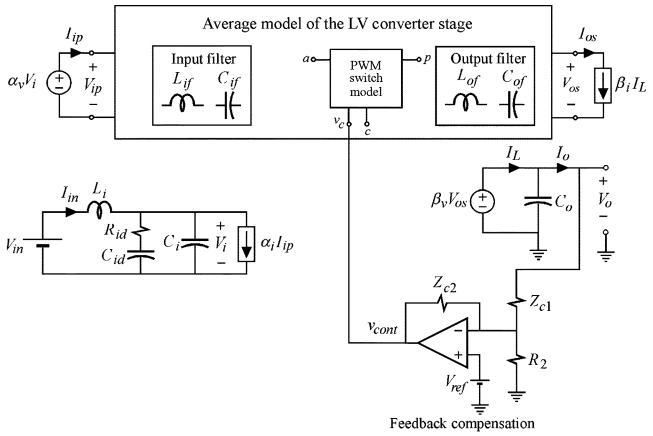


Fig. 16. Reduced average model of an MV converter obtained from the real-time reduced model in Fig. 11 by the use of the appropriate PWM switch.

external ramp S_e in the current feedback loop as will be explained in the next section. In both isolated boost converters in Figs. 5 and 6, the magnetizing inductance of the isolation transformer has no effect at all in the average circuit model shown in Fig. 17(b). The magnetizing inductance of the isolation transformer of the Cuk converter in Fig. 8 has significant effect on the average small-signal model and its effect is compensated by the addition of damping network across C_1 [14]. In all these average models, the small capacitor C_ε and its damping network at the input of the output is ignored.

As a specific example, the reduced average model of the 10 kV-to-400 V converter obtained from the real-time reduced model in Fig. 12 using the PWM switch model is shown in Fig. 18. Since peak current-mode control is used in Fig. 12, the model of the CC-PWM is used. The necessary parameters

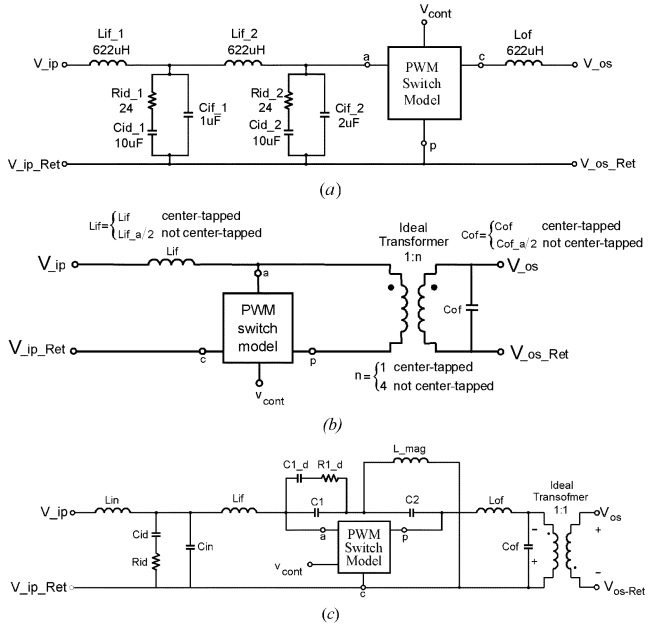


Fig. 17. Average circuit models of the (a) buck, (b) boost, and (c) Cuk LV converter stages used in Fig. 16.

that must be supplied to the CC-PWM are shown in Fig. 18 and will be discussed in more detail in the next section. In Fig. 18 we see the output voltage of the error amplifier, which is the control signal, has been multiplied by two because of the way the external ramp is implemented in Fig. 12 as explained earlier. This average model will be used to determine the large signal dynamic response and the small-signal loop gain. The results obtained from both models and the hardware will be compared in Section XII.

XI. Loop-Gain Analysis and Feedback Compensation

The parameters supplied to the large-signal average model of the CC-PWM switch in Fig. 14 are the following.

a) *The switching frequency*, F_s: In the forward and Cuk converters, F_s is the same as the switching frequency of the switches. In both isolated boost converters, F_s is twice the frequency that the switches operate at.

b) *The current-sense trans-resistance* R_i: This is the current-to-voltage conversion factor of the current sense signal in the switches on the primary side. In the Cuk and forward converters, the current in only one of the switches on the primary side needs to be sensed, but in both boost converters the sum of the current in both switches need to be sensed. A practical way to sense the sum of the current in both switches is to place the current sense in the return path to the input source common to both switches.

c) *The external ramp* S_e: This is a ramp voltage signal added to current-sense signal to stabilize against subharmonic oscillations. In the forward converter, the magnetizing current of the isolation transformer forms part of the external ramp added to the current sense signal. Often, the magnetizing current is small in comparison to the actual output inductor current and can be ignored. If not

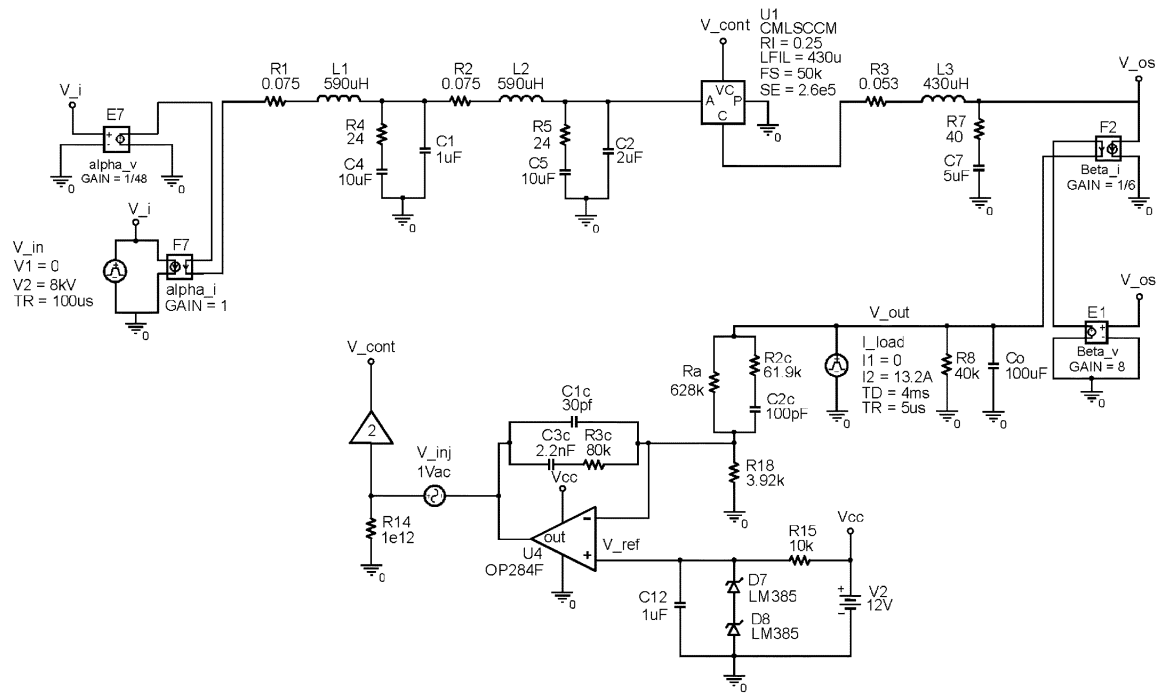


Fig. 18. Reduced average model of the MV-to-LV converter obtained by the use of the model of the CCPWM switch.

ignored, then the component of the external ramp due to the magnetizing current is

$$S_{e\_M} = \frac{V_{\rm ip}}{L_M} R_i, \quad \text{forward converter.} \tag{60}$$

In the Cuk converter, the magnetizing current contributes a negative external ramp which is given by

$$S_{e\_M} = -\frac{V_{\rm ip}}{L_M} R_i, \quad \text{Cuk converter.} \tag{61}$$

In both types of isolated boost converters, the magnetizing current of the isolation transformer has no effect on the external ramp.

d) *The total switched inductance L*: For the forward, boost, and Cuk converters, L is given by

$$L = \begin{cases} L_{\rm of}, & \text{buck (forward)} \\ L_{\rm if}, & \text{boost} \\ L_{\rm of} \,||\, L_{\rm if}, & \text{Cuk} \end{cases} \tag{62}$$

where $L_{\rm of}$ and $L_{\rm if}$ are shown in Figs. 17(a), (b) and (c). The value of L is used to compute the value of C_s in the model of CC-PWM according to

$$C_s = \frac{4}{\omega_s^2 L}; \quad \omega_s = 2\pi F_s. \tag{63}$$

The resonance formed by L and C_s models the subharmonic response of peak current-mode control.

The loop gain is determined analytically from the circuit model in Fig. 16. When peak current mode control is used, then the small-signal parameters of the PWM switch are those of the CC-PWM switch evaluated at the dc operating point $(I_c, D, V_{\rm ap})$ and given by

$$\begin{aligned} k_o &= \frac{1}{R_i}\frac{I_c}{|I_c|} \\ g_o &= \frac{T_s}{L}\left(D'\frac{S_e}{S_n} + \frac{1}{2} - D\right) \\ g_f &= Dg_o - \frac{DD'T_s}{2L} \\ g_i &= -\frac{DI_c}{V_{\rm ap}} \\ g_r &= \frac{I_c}{V_{\rm ap}} \end{aligned} \tag{64a-e}$$

where

$I_c =$ dc value of the common-terminal current.
$V_{\rm cp} =$ dc value of the voltage at port cp.
$V_{\rm ap} =$ dc value of the voltage at port ap.
$D = \dfrac{V_{\rm cp}}{V_{\rm ap}} =$ dc value of duty cycle.
$S_n = \dfrac{V_{\rm ap} - V_{\rm cp}}{L} R_i =$ dc value of the natural ramp of the inductor current during the on time.
$R_i =$ equivalent current−sense resistance. (65a-f)

As an example, we will analytically determine the loop gain of the MV-to-LV converter using the circuit model in Fig. 18 in which the small-signal model of the CC-PWM switch is used. First, the dc operating point of the CC-PWM switch is determined in terms of the dc quantities of the converter as follows:

$I_c = I_o$ dc output current.
$V_{\rm cp} = V_o$ dc output voltage
$V_{\rm ap} = V_{\rm in}$ dc input voltage
$D = \dfrac{V_o}{V_{\rm in}} =$ dc value of duty cycle. (66a-d)

The analytical determination of the control-to-output transfer function of the circuit in Fig. 18 is tedious because of the presence of the six-order input filter in addition to the third-order main power stage $(C_s, L_{\rm of}, C_o)$. For a first cut design, it is not necessary however to carry this analysis in its entirety because the output impedance of the properly damped input filter is very low and can be ignored. Hence, we begin by determining the control-to-output transfer function without the input filter, which can be shown to be given by

$$G(s) = G_o \frac{1+s/\omega_z}{1+s/\omega_p} \frac{1}{1+s/(\omega_n Q_n)+s^2/\omega_n^2} \tag{67}$$

in which

$$\begin{aligned} G_o &= \frac{\beta_v k_o R_L}{1+g_o R_L} \\ \omega_z &= \frac{1}{r_c C_o \beta_v \beta_i} \\ \omega_p &= \frac{1+g_o R_L}{R_L C_o \beta_v \beta_i} \\ \omega_n &= \frac{\omega_s}{2} \\ Q_n &= \frac{1}{\omega_n L_{\rm of} g_o}. \end{aligned} \tag{68a-e}$$

Note that the product $G_o\omega_p$ is independent of the input voltage and is given by

$$G_o \omega_p = \frac{k_0}{C_o \beta_i}. \tag{69}$$

It follows that the crossover frequency of the loop gain will also be nearly independent of the input voltage.

The transfer function of the error amplifier in Fig. 18 is given by

$$H(s) \equiv \frac{v_c(s)}{v_o(s)} = H_o \frac{(1+\omega_{z1}/s)(1+s/\omega_{z2})}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \tag{70}$$

in which

$$\begin{aligned} H_o &= \frac{R_{3c}}{R_a} \frac{2}{1+C_{1c}/C_{3c}} \approx \frac{2R_{3c}}{R_a} \\ \omega_{z1} &= \frac{1}{R_{3c}C_{3c}} \\ \omega_{z2} &= \frac{1}{(R_{2c}+R_a)C_{2c}} \approx \frac{1}{R_a C_{2c}} \\ \omega_{p1} &= \frac{1}{R_{3c}C_{1c}||C_{3c}} \approx \frac{1}{R_{3c}C_{1c}} \\ \omega_{p2} &= \frac{1}{R_{2c}C_{2c}}. \end{aligned} \tag{71}$$

The loop gain without the input filter is then given by

$$\begin{aligned} T(s) &= G(s)H(s) \\ &= T_o \frac{1+s/\omega_z}{1+s/\omega_p} \frac{(1+\omega_{z1}/s)(1+s/\omega_{z2})}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \frac{1}{\Delta(s)} \end{aligned} \tag{72}$$

in which

$$T_o = G_o H_o \tag{73}$$

$$\Delta(s) = 1 + s/(\omega_n Q_n) + s^2/\omega_n^2. \tag{74}$$

The objective is to determine the compensation poles and zeros so that $T(j\omega)$ crosses over with adequate phase margin at about a tenth of the switching frequency. The two poles, ω_{p1} and ω_{p2}, are placed considerably beyond the crossover frequency somewhere between half the switching frequency and the switching frequency. The purpose of these poles is to attenuate spikes associated with the switching frequency which may interfere with the PWM process downstream from the error amplifier. The zero, ω_z, can be ignored because it occurs at frequencies well above the switching frequency when high grade capacitors, such as supermetalized polypropylene or ceramic, are used. The quadratic factor $\Delta(\rm s)$ occurs at half the switching frequency and has a Q-factor which is damped by the external ramp and given by

$$\begin{aligned} Q_n &= \frac{1}{\omega_n L_{\rm of} g_o} \\ &= \frac{1}{\pi} \frac{1}{D' \frac{S_e}{S_n} + \frac{1}{2} - D}. \end{aligned} \tag{75}$$

A conservative choice of the ratio of the external ramp to the natural ramp in (75) is two when the natural ramp is at its steepest at maximum input voltage. For the present design in Fig. 18, this ratio is about 2.83 when the input voltage is 10 kV and 6.88 when the input voltage is at 5.5 kV. The value of Q_n then falls in the range $0.081 < Q_n < 0.132$ so that the quadratic factor can be approximately factored as

$$\Delta(s) \approx \left(1 + \frac{s}{Q_n \omega_n}\right)\left(1 + \frac{s}{(\omega_n/Q_n)}\right). \tag{76}$$

The second pole in (76) falls well above the frequency range of interest and can be ignored in an approximate analysis. Hence, up to the crossover frequency, the useful loop gain can be approximated as follows:

$$T(s) \approx T_o \frac{(1+\omega_{z1}/s)(1+s/\omega_{z2})}{(1+s/\omega_p)(1+s/(\omega_n Q_n))}. \tag{77}$$

To determine an analytical expression of the crossover frequency, all we need is the behavior of the magnitude of the loop gain in (77) near the crossover. The crossover is always chosen significantly above the dominant pole $f_p = \omega_p/2\pi$, which for all operating conditions is below 300 Hz, as can be verified from (68c). The first zero, ω_{z1}, is placed below the crossover frequency and above ω_p in order to ensure a slope of -20 dB/dec near crossover while maintaining good settling time. Similarly, the second zero, ω_{z2}, is placed in the middle of the range of the second pole in (77), which is given by $2.0\ \text{kHz} < f_n Q_n < 3.3\ \text{kHz}$, at

$$f_{z2} = \frac{1}{2\pi} \frac{1}{(628\ \text{k}\Omega)(100\ \text{pF})} = 2.5\ \text{kHz}.$$

It follows that the loop gain in (77) near the crossover can be approximated as

$$T(s) \approx \frac{T_o \omega_p}{s} \frac{\omega_n Q_n}{\omega_{z2}} = \frac{\omega_x}{s} \tag{78}$$

in which ω_x is a very good approximation of the angular crossover frequency given by

$$\omega_x = T_o \frac{\omega_p \omega_n}{\omega_{z2}}. \tag{79}$$

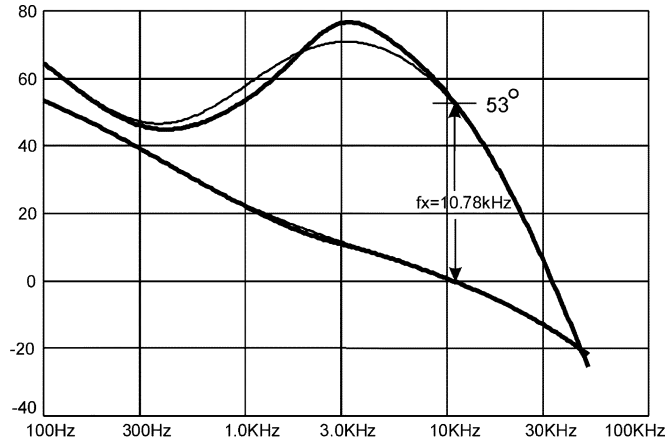


Fig. 19. Loop gain and phase with (thick trace) and without (thin trace) the input filter at an input voltage of 8 kV and load current of 12.5 A obtained from the simulation circuit in Fig. 18.

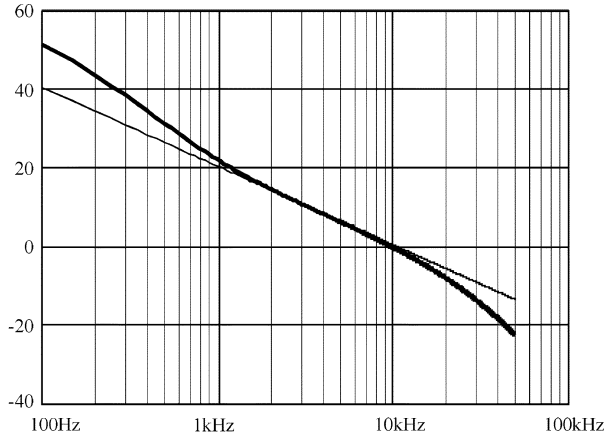


Fig. 20. Comparison of the approximate (thin trace) and exact (thick trace) expressions of the loop gain. Near the cross-over frequency both expressions are very nearly the same.

After performing the necessary substitutions in (79), the following analytical expression of the crossover frequency is obtained:

$$f_x = \frac{1}{2\pi}\frac{H_o}{\beta_i R_i C_o \omega_{z2}}\frac{F_s}{\frac{1}{\alpha_v\beta_v}\frac{V_o}{V_{\rm in}}\left(\frac{S_e L_{\rm of}\beta_v}{V_o R_i}-1\right)+\frac{1}{2}}. \quad (80)$$

To determine the phase margin at the crossover frequency, we need to determine the additional phase shift of the high-frequency poles at the crossover frequency as follows:

$$\begin{aligned}\phi_M &= 180^\circ - \left[90^\circ + \tan^{-1}\frac{f_x}{f_{p1}} + \tan^{-1}\frac{f_x}{f_{p2}}\right] \\ &= 90^\circ - \tan^{-1}\frac{f_x}{f_{p1}} - \tan^{-1}\frac{f_x}{f_{p2}}. \end{aligned} \quad (81)$$

A numerical verification of the results derived above is given next. First, we show in Fig. 19 that the loop gain obtained from the simulation model in Fig. 18 with and without the input filter are essentially the same. The crossover frequency and the phase margin in Fig. 19 are seen to be 10.78 kHz and 53°, respectively. Next, we compare the approximate and exact expressions of the loop gain in (78) and (72) in Fig. 20 in which we see that both loop gains essentially cross over at the same frequency. Hence, we compute the approximate crossover frequency and phase margin using (80) and (81)

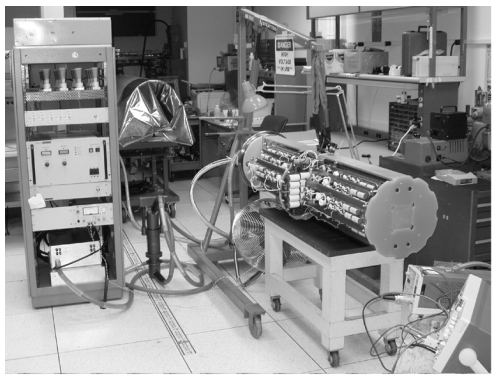
$$\begin{aligned} f_x &= \frac{1}{2\pi}\frac{0.251}{(0.167)(0.25\,\Omega)(100\,\mu{\rm F})(15.92\,{\rm krad/s})} \\ &\quad\times\frac{50\ {\rm kHz}}{\frac{1}{(0.021)8}\frac{400\ {\rm V}}{8000\ {\rm V}}\left(\frac{(2.6\times10^5\ {\rm V}/s)(430\ \mu{\rm H})8}{400\ {\rm V}(0.25\ \Omega)}-1\right)+\frac{1}{2}} \\ &= 10.45\ {\rm kHz} \end{aligned}$$

$$\phi_M = 90^\circ - \tan^{-1}\frac{10.45\ {\rm kHz}}{25.71\ {\rm kHz}} - \tan^{-1}\frac{10.45\ {\rm kHz}}{64.18\ {\rm kHz}} = 58.5^\circ.$$

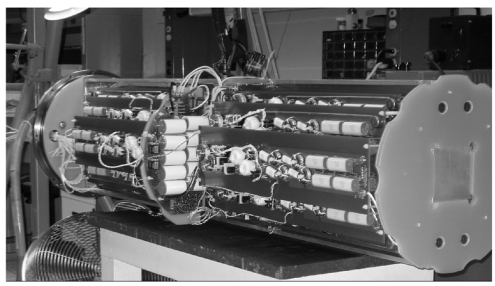
Both of these approximate calculations are seen to be close to the exact simulation results.

XII. Experimental Results

Following recommendations of initial reliability analyses, it was decided that two 10 kV-to-400 V converters, shown in Fig. 21, should be built for redundancy purposes for the Monterey Bay Aquarium Research Institute (MBARI) underwater observatory which is to serve as a test bed for the more ambitious Neptune project [1]. The converters shown are enclosed in a cylindrical vessel filled with Flourinert (FC-77) which is a liquid that prevents corona in the power transformers and provides cooling. When test results from the 16-stage prototype became available and the results of the reliability analysis were refined, the highly redundant and reliable nature of the MV converter was established and the need for a second redundant converter was dropped by Alcatel [9]. As the program at JPL came to an abrupt end, the tests that could be done on the converter became limited to testing in open air, rather than



(*a*)



(*b*)

Fig. 21. (a) Laboratory setup. (b) Converter assembly with two redundant converters.

in Fourinert, which in turn limited the output power to 5 kW (instead of 10 kW) and the input voltage to -8 kV (instead of -10 kV). It is the results of these tests which are reported here. Fortunately, sufficient care was exercised in following high voltage practices on the packaging of the converter from a spacing point of view. The gate-drive and power transformers were designed to withstand 12-kV dc isolation. The gate-drive transformers were potted while the power transformers relied on Flourinert. The start-up circuit used in this converter is discussed in [12]. It is to be noted that the input voltage for the MBARI and NEPTUNE projects is negative because power is transmitted to the ocean floor using a *single* cable and returned through earth by grounding electrodes which must be positive in order to prevent erosion.

A. Verification of Voltage and Current Sharing and Redundancy

A 16-stage prototype with stacking configuration $[16, 1] \rightarrow [8, 2]$, operating from -3.3 kV input voltage and delivering 0 to 5 A at 400 V, was subjected to destructive testing by inducing a failure in one of the converter stages by shorting each of its four power MOSFETs, one at a time. Each failure was induced under four different operating scenarios as follows. In one set of tests, the converter was powered up with a shorted MOSFET at full load and no load. In another set of tests, a MOSFET was shorted while the converter was in operation at full load and no load. In all these tests, the output voltage of the failed stage went from 50 to 0 V while the output voltages of the remaining stages in the stack went from 50 to $50\ \mathrm{V} + 50/7 = 57.1$ V. The current in both stacks always remained the same. The input current and the efficiency of the converter remained the same before and after the failure. Hence, it was conclusively demonstrated that the failure of one converter stage had no effect on the overall converter performance.

Sharing of the voltages and currents in steady state as well as during start-up and dynamic load transients was demonstrated on the full 48-stage converter at an input voltage of -8 kV. The output voltages, with respect to output return, of the second, third and fourth stages from the six stacks are tabulated at four different load settings in Table I which indicate excellent sharing among the various stages in all the stacks in steady state. In Fig. 22, the output voltages, with respect to output return, of the second, third and fourth stages from the first, third and sixth stacks respectively also indicate perfect sharing during the start-up transient of the converter. Fig. 23 shows that the output voltages of the second and fourth stages during a 0-to-13.2 A dynamic load transient maintain excellent sharing while the (inductive) current in the third stack is seen to reach an average value exactly equal to one sixth of the total load current, i.e., $2.2\ \mathrm{A} = 13.2\ \mathrm{A}/6$.

The output voltage ripple over the entire output load range is about 230 mV (0.05%) at $V_{\mathrm{in}} = -8$ kV and is shown in Fig. 24. The output voltage and input current during start-up into 5-kW load is shown in Fig. 25.

Finally, the converter demonstrated an efficiency of 90%–91% over the input voltage and load range which is the same as the efficiency of any one of the 48 subconverters.

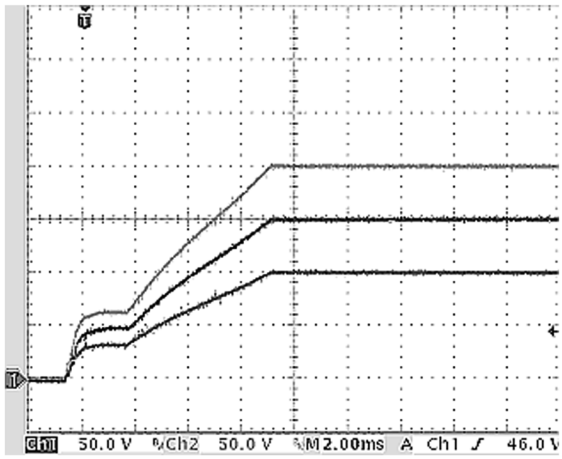


Fig. 22. Stack voltages during start up at no load and $V_{\mathrm{in}} = -8$ kV. Top trace: fourth converter from bottom in sixth stack. Middle trace: third converter from bottom in third stack. Bottom trace: second converter from bottom in first stack. Scale 50 V/div and 2 ms/div.

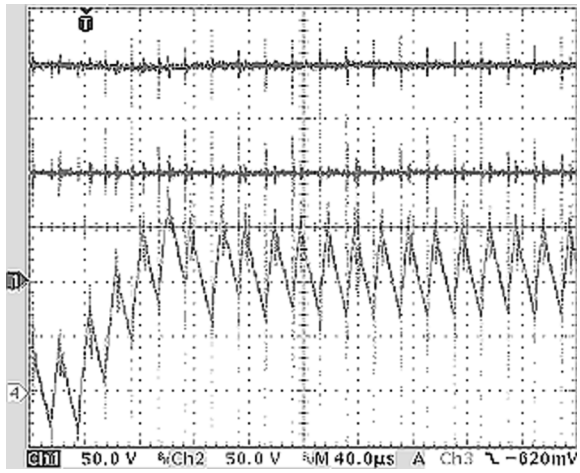


Fig. 23. Dynamic load response of the current (bottom trace) going into the third stack, the voltage of the fourth stage in the sixth stack (top trace) and the voltage of the second stage in the first stack (middle trace) for a 0–13.2 A step load with $V_{\mathrm{in}} = -8$ kV. Scale 1 A/div and 50 V/div. The stack voltages are seen to remain at 100 and 200 V while the current going in the third stack is seen to reach an average value of $13.2\ \mathrm{A}/6 = 2.2$ A in about 80 μs. This demonstrates perfect sharing of voltages and currents, even under large transient conditions, throughout the 48 stages of the MV-to-LV converter.

B. Verification of the Real-Time and Average Reduced Models

The predicted waveforms obtained from the real-time and average models, shown in Figs. 12 and 18, respectively, are given in Figs. 26–28 and will be compared to the measurements. The value of the resistor used in the compensation network, R_{3c}, in the actual hardware was 160 K instead of 80 K, which sets the crossover frequency at about 13.4 kHz with a phase margin of 39 degrees. This is a rather high crossover frequency for a converter operating at 50 kHz and is generally *not* recommended. The predictions of the real-time and average reduced models of the measured inductor current in Fig. 23 is shown in Fig. 26. The prediction of the real-time model is seen to be in very good agreement with the measurement while that of the average model is seen to be quite acceptable. There are two reasons for some of the apparent discrepancies in the average model with a *fast control*

TABLE I
OUTPUT VOLTAGE AND STACK VOLTAGES FOR FOUR DIFFERENT LOADS AT $V_{\rm in} = -8$ KV. THE VOLTAGE SHARING IS SEEN TO BE EXCELLENT

V_{out}	402.4V	402.5V	402.5V	402.5V
P_{out}	0kW	1.27kW	2.02kW	4.9kW
2nd stage/stack 1	99.73V	99.62V	99.55V	99.17V
3rd stage/stack 2	152.9V	153.0V	153.0V	152.8V
3rd stage/stack 3	151.4V	151.4V	151.4V	150.98V
3rd stage/stack 4	150.6V	150.6V	150.6V	150.19V
3rd stage/stack 5	148.2V	148.2V	148.1V	147.65V
4th stage/stack 6	198.9V	199.1V	199.12V	199.21V

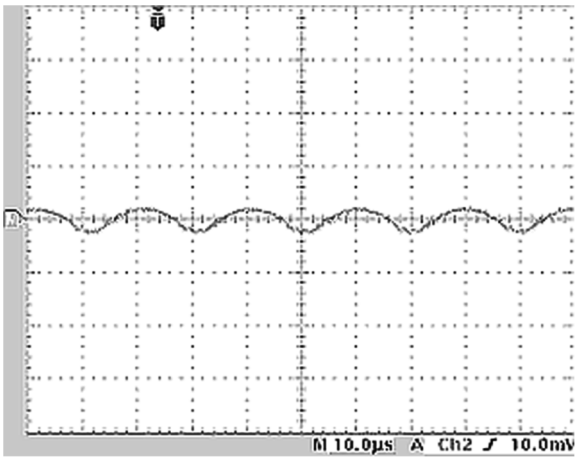


Fig. 24. Ripple component of the output voltage at no load and at full load at $V_{\rm in} = -8$ kV. Scale 500 mV/div and 10 μs/div.

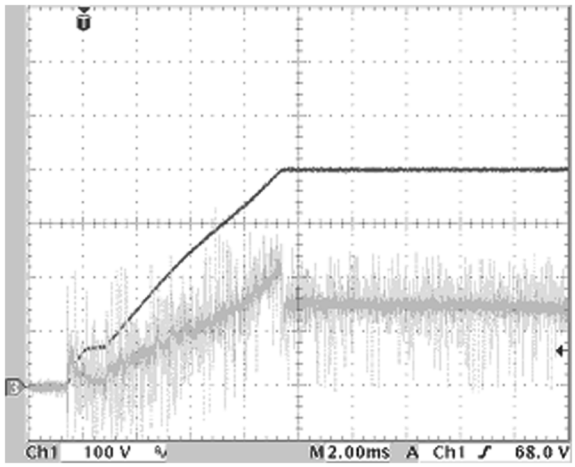


Fig. 25. Start-up input current and output voltage at a load of 5.0 kW and $V_{\rm in} = -7$ kV. Scale; 100 V div, 500 mA/div, and 2 ms/div.

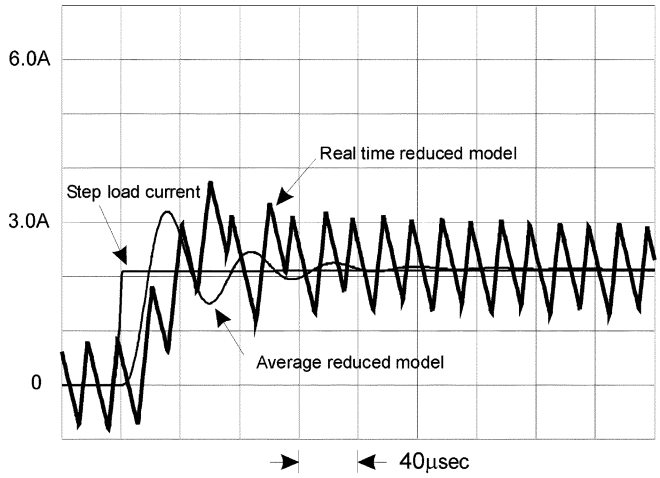


Fig. 26. Predicted response of the inductor current using the real-time and average reduced models in Figs. 12 and 18, respectively. The applied step load current is shown in the thin blue trace. The agreement of the real-time prediction with the measured waveform in Fig. 23 is excellent.

loop such as the one we have here. First, the duty cycle of the actual converter (and the real-time reduced model) cannot exceed 45% whereas in the average model the duty cycle is a continuous function which can take on *any* value (even larger than unity). Second, the actual converter cannot make any meaningful corrections to the output voltage on time scales shorter than the switching period whereas the average model can. This means that, *if the loop is fast enough*, the average model can always make *bigger and faster* corrections to any disturbance than the actual converter or the real-time model. This is further illustrated by the response of the output voltage to dynamic load changes as will be explained next.

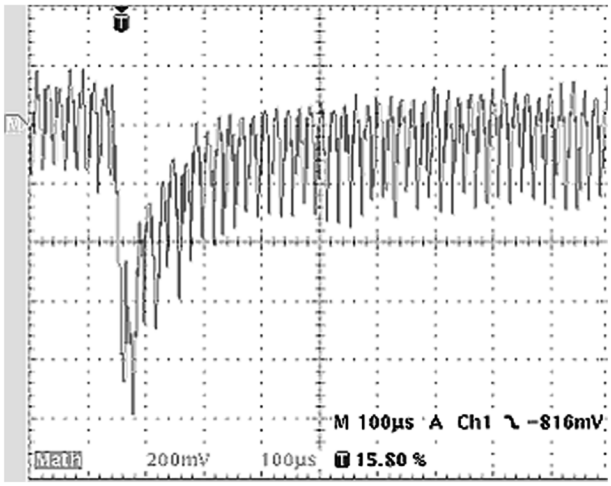
Figs. 27(a) and (b) show the measured and predicted output voltage response to a dynamic load change of only 0-to-4.9 A and at an input voltage of -8 kV. Once again the agreement between the real-time reduced model and the actual measurement is very good while the prediction of the average model is reasonably good. The agreement between the average model and measurement deteriorates when the step load current is increased to 0-to-13.2 A as shown in Fig. 28. The main discrepancy in the average model is the peak undershoot in the output voltage which to an excellent approximation is given by

$$\Delta V = \frac{\Delta I}{2\pi f_x C_o} \tag{82}$$

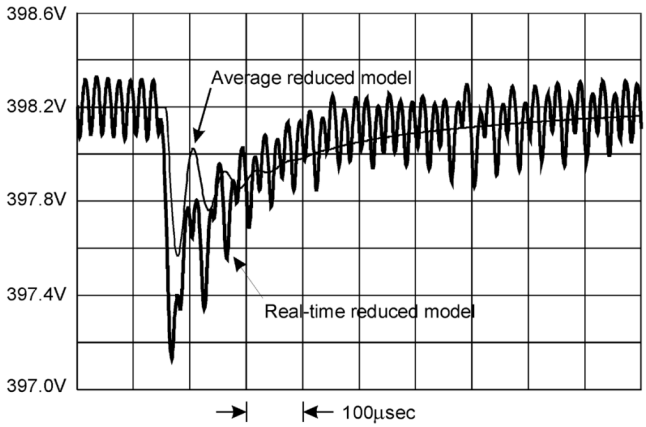
in which

$$\begin{aligned} \Delta I &\equiv \text{magnitude of the step load current} \\ \Delta V &\equiv \text{peak overshoot or undershoot} \\ f_x &\equiv \text{crossover frequency.} \end{aligned} \tag{83}$$

When this expression is evaluated for 4.9 A and 13.2 A steps, we obtain ΔV of 590 mV and 1.6 V, respectively. These numbers are seen to be in close agreement with results of the average model in Figs. 27 and 28. Since the duty cycle can narrow down to zero with no limitation in the actual converter and the average model, the peak overshoot of the average model and that of the real-time model or measurement agree very well, as shown in Fig. 29. The rise time of the dynamic load current, in addition to its amplitude, is another contributing factor to the response of the output voltage *with a very fast control loop*. The actual rise time in the experimental circuit was not known but when a

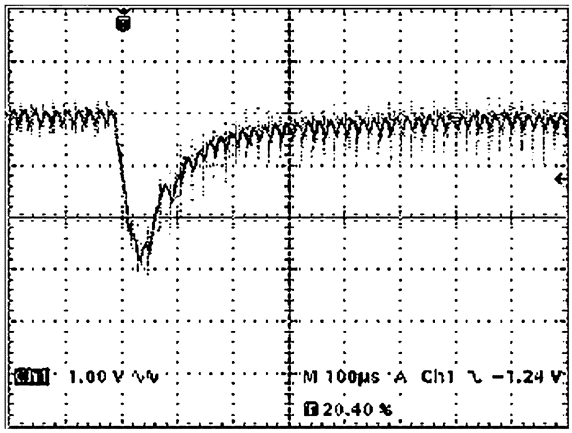


(a)

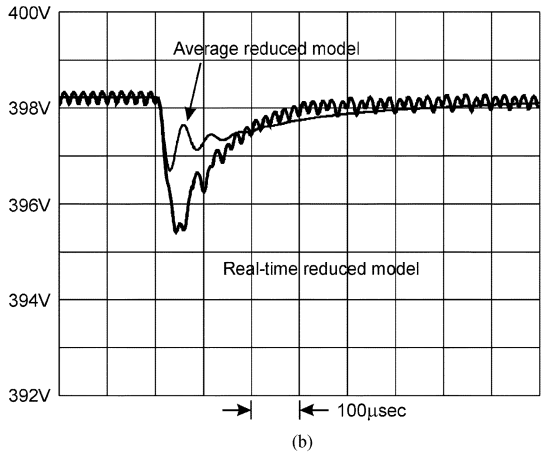


(b)

Fig. 27. (a) Output voltage response to a 0-to-4.9 A dynamic load at $V_{\rm in} = -8$ kV and (b) the predicted response obtained from the reduced real-time and average models in Figs. 12 and 18, respectively.



(a)



(b)

Fig. 28. (a) Output voltage response to a 0-to-4.9 A dynamic load at $V_{\rm in} = -8$ kV and (b) the predicted response obtained from the reduced real-time and average models in Figs. 12 and 18, respectively.

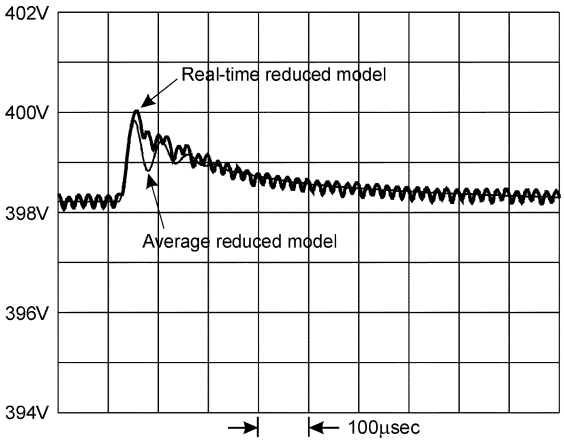


Fig. 29. Agreement between the average and real-time models is very good when the converter is step unloaded 13.2 A-to-0 A because there is no limitation on the narrowing of the duty cycle.

rise time of about 13.2 A/20 μs was chosen in the real-time reduced model the best agreement between experiment and simulation was obtained as can be seen. If the loop is slow, i.e., the crossover frequency is less than 5% of the switching frequency, then agreement between the average model and the actual converter or the real-time model is always very good. This is shown by selecting $R_{3c} = 10\ \text{k}\Omega$ and $C_{3c} = 0.033\ \mu$F in the feedback circuit so that the crossover frequency is 1.2 kHz and the phase margin 72 degrees. The resulting response of the output voltage to a dynamic load of 0-to-13 A predicted by the average and real-time models is shown in Fig. 30. The peak undershoot is seen to be in excellent agreement with (82).

XIII. Conclusion

A simple and systematic method of synthesis of highly redundant MV power converters using low-voltage, high frequency PWM converters has been presented and demonstrated using a −10 kV-to-400 V, 10-kW prototype. Accurate analytical models are given to facilitate the design and simulation of these converters in closed-loop operation.

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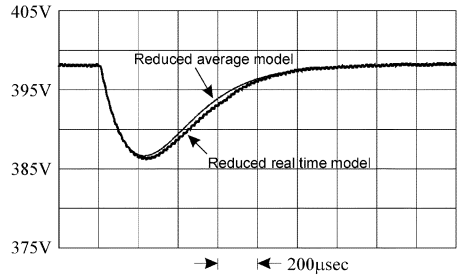

Fig. 30. Agreement between the average and real-time models is very good under all conditions when the cross-over frequency is selected considerably below the switching frequency at 1.2 kHz. Shown here is the response of the output voltage to a dynamic load step of 0-to-13.2 A.

project, especially when funds became scarce during the final days of the project at JPL.

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